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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

CLASS U.S. PTO
10/003304
12/06/01

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|----------------------|-------------|-------|----------|------|----------|
| APPLICATION | FILING DATE | CLASS | SUBCLASS | GAU | EXAMINER |
| APPL NUM 10003304 | 01/17/2002 | 257 | 3 | 2811 | N11 |

**APPLICANTS: Nakamura Shunji:

**CONTINUING DATA VERIFIED:

THIS APPLICATION IS A DIV OF 08/970,212 11/14/1997

** FOREIGN APPLICATIONS VERIFIED:

JAPAN 07-137968/1995 06/05/1995

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|--|---|----------------------------------|-------------------------------|
| PG-PUB | DO NOT PUBLISH <input type="checkbox"/> | RESCIND <input type="checkbox"/> | ATTORNEY DOCKET NO 960456B |
| Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no | | | |
| 35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no | | | |
| Verified and Acknowledged Examiners's initials | | | |
| TITLE : Semiconductor memory device and method for fabricating the same | | | |

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436 (Rev. 12-94)

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|--|-----------|----------------------------|-----------------------------|----------------------|
| NOTICE OF ALLOWANCE MAILED | | Assistant Examiner | CLAIMS ALLOWED | |
| | | | Total Claims | Print Claim for O.G. |
| ISSUE FEE | | Primary Examiner | DRAWING | |
| Amount Due | Date Paid | | Sheets Drwg. | Figs. Drwg. |
| <input type="checkbox"/> TERMINAL DISCLAIMER | | PREPARED FOR ISSUE: | Application Examiner | |
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